REMARKS

Claims 1-38 are pending in this application. Claims 1-2, 4, 6, 8, 11, 12, 14, 16, 18, 21, 22, 24, 26, and 28 have been amended in several particulars for clarity and brevity while Claims 31-38 have been newly added to alternatively define Applicants' disclosed invention in accordance with current Office policy, to expedite compact prosecution of the instant application. A fee of $224.00 is incurred by the addition of one independent claim and eight (8) claims in excess of twenty (20). Separately, formal drawings are submitted herewith for the Examiner's convenience.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be in condition for examination. Should any questions remain unresolved, the Examiner is requested to telephone Applicant's attorney at (703) 312-6600.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 of Antonelli, Terry, Stout & Kraus, LLP (referencing Attorney Docket No. 219.39515X00), and please credit any excess fees to said deposit account.

Attached hereto is a marked-up version of the changes made to the claims. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS

Claims 1-2, 4, 6, 8, 11, 12, 14, 16, 18, 21, 22, 24, 26, and 28 have been **amended**, and claims 31-38 have been newly **added** as follows:

1. (Amended) A functional random instruction testing (FRIT) method for testing a complex device, comprising:

[~~generating a FRIT kernel;~~]

converting [~~the~~] FRIT kernel into kernel test patterns and storing the kernel test patterns in a tester memory;

loading, at the tester, the kernel test patterns stored in the tester memory onto an on-board memory of a complex device under test (DUT);

executing, at the complex device under test (DUT), a re-generative functional test of the complex device under test (DUT) by applying the kernel test patterns to the complex device under test (DUT); and

comparing, at the tester, a test result of the re-generative functional test with [~~a test~~] an expected test result to check for manufacturing defects.

2. (Amended) The method as claimed in claim 1, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test

of the complex device under test (DUT), and the expected test result obtained from computer modeling of the complex device under test (DUT).

4. (Amended) The method as claimed in claim 2, wherein said software built-in self-test engine (SBE) of the FRIT kernel comprises:

a RIT generator [~~configured with~~] including compact RIT machine code [~~that can~~] reside in the on-board memory of the complex device under test (DUT) for generating the re-generated functional test;

a test program execution module [~~configured with~~] including test execution directives for providing an environment to store and run the re-generated functional test; and

a test result compaction module [~~configured with~~] including compression machine code [~~that compresses~~] to compress test results of the re-generated functional test for storage in the on-board memory of the complex device under test (DUT).

6. (Amended) The method as claimed in claim 1, wherein said complex device under test (DUT) [indicates] includes a microprocessor.

8. (Amended) The method as claimed in claim 7, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test of the complex device under test (DUT), and the expected test result obtained either from computer modeling of the complex device under test (DUT) or from a known good device.

11. (Amended) A computer readable medium having stored thereon a functional random instruction test (FRIT) kernel which, when executed by a [~~tester~~] system, cause the [~~tester~~] system to perform:

receiving the FRIT kernel in kernel test patterns and storing the kernel test patterns in a tester memory;

loading the kernel test patterns stored in the tester memory onto an on-board memory of a complex device under test (DUT);

enabling execution, at the complex device under test (DUT), a re-generative functional test of the complex device under test (DUT) by applying the kernel test patterns to the complex device under test (DUT); and

making a comparison between a test result of the re-generative functional test and [~~a test~~] an expected test result to check for manufacturing defects.

12. (Amended) The computer readable medium as claimed in claim 11, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test of the complex device under test (DUT), and the expected test result.

14. (Amended) The computer readable medium as claimed in claim 12, wherein said software built-in self-test engine (SBE) of the FRIT kernel comprises:

a RIT generator [~~configured with~~] including compact RIT machine code [~~that can~~] in the on-board memory of the complex device under test (DUT) for generating the re-generated functional test;

a test program execution module [~~configured with~~] including test execution directives for providing an environment to store and run the re-generated functional test; and

a test result compaction module [~~configured with~~] including compression machine code [~~that compresses~~] to compress test results of the re-generated functional test for storage in the on-board memory of the complex device under test (DUT).

16. (Amended) The computer readable medium as claimed in claim 11, wherein said complex device under test (DUT) [~~indicates~~] includes a microprocessor.

18. (Amended) The computer readable medium as claimed in claim 17, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test of the complex device under test (DUT), and the expected test result obtained from computer modeling of the complex device under test (DUT) or from a known good device.

21. (Amended) A test system for testing a complex device, comprising:

a complex device under test (DUT) having an on-board memory; and

a tester including a tester memory [~~arranged~~]to test a functionality of the complex device under test (DUT) by:

receiving the FRIT kernel in kernel test patterns and storing the kernel test patterns in the tester memory;

loading the kernel test patterns stored in the tester memory onto the on-board memory of the complex device under test (DUT);

enabling execution, at the complex device under test (DUT), a re-generative functional test of the complex device under test (DUT) by applying the kernel test patterns to the complex device under test (DUT); and

making a comparison between a test result of the re-generative functional test and [~~a test~~] an expected test result to check for manufacturing defects.

22. (Amended) The test system as claimed in claim 21, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test of the complex device under test (DUT), and the expected test result.

24. The test system as claimed in claim 22, wherein said software built-in self-test engine (SBE) of the FRIT kernel comprises:

a RIT generator [~~configured with~~] including compact RIT machine code [~~that can~~] in the on-board memory of the complex device under test (DUT) for generating the re-generated functional test;

a test program execution module [~~configured with~~] including test execution directives for providing an environment to store and run the re-generated functional test; and

a test result compaction module [~~configured with~~] including compression machine code [~~that compresses~~] to compress test results of the re-generated functional test for storage in the on-board memory of the complex device under test (DUT).

26. (Amended) The test system as claimed in claim 21, wherein said complex device under test (DUT) [~~indicates~~] includes a microprocessor.

28. (Amended) The test system as claimed in claim 27, wherein said FRIT kernel includes a software built-in self-test engine (SBE) [~~configured~~] to execute the re-generative functional test of the complex device under test (DUT), and the expected test result obtained from computer modeling of the complex device under test (DUT) or from a known good device.

--**31.** A complex device, comprising:

a memory to store a functional random instruction testing (FRIT) kernel in kernel test patterns; and

a processor to perform a re-generative functional test of the complex device under test (DUT) upon execution of the kernel test patterns and to enable comparison between a test result of the re-generative functional test and an expected test result to check for manufacturing defects.

32. The complex device as claimed in claim 31, wherein said FRIT kernel includes a software built-in self-test engine (SBE) to execute the re-generative functional test of the complex device under test (DUT), and the expected test result.

33. The complex device as claimed in claim 32, wherein said expected test result is obtained from computer modeling of the complex device under test (DUT) or from a known good device.

34. The complex device as claimed in claim 32, wherein said software built-in self-test engine (SBE) of the FRIT kernel comprises:

a RIT generator including compact RIT machine code to reside in the on-board memory of the complex device under test (DUT) for generating the re-generated functional test;

a test program execution module including test execution directives for providing an environment to store and run the re-generated functional test; and

a test result compaction module including compression machine code to compress test results of the re-generated functional test for storage in the on-board memory of the complex device under test (DUT).

35. The complex device as claimed in claim 32, wherein said test execution environment employs an exception handler for handling illegal conditions such as undesirable memory accesses, deadlock, shut-down, and infinite loops.

36. The complex device as claimed in claim 32, wherein, when the kernel test patterns are applied to the processor from the memory, the processor performs the following:

beginning a set-up for executing the kernel test patterns;

executing the kernel test patterns to generate a series of test sequences and associated data for respective test sequences;

running the test sequences, and at the end of the test sequences, obtaining the test results for storage in the on-board memory; and

dumping the test results of the kernel test patterns to the tester, via an interface, for enabling said comparison with the expected test result to check for manufacturing defects.

37. The complex device as claimed in claim 32, wherein said software built-in self-test engine (SBE) of the FRIT kernel is programmed to generate and execute one or more ("N") instruction sequences, each sequence being executed on one or more (M) data sets where N and M represent an integer no less than "1" and are user-specified numbers used in generating the FRIT kernel by an especially designed software tool.

38. The complex device as claimed in claim 37, wherein said software built-in self-test engine (SBE) of the FRIT kernel is further programmed to generate one or more signatures to provide a unique identification of the test result of each test sequence and indicate whether the test result of a particular test sequence is “good” or “bad”.--